REMARKS

The Examiner objected to the drawings, stating "The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the top electrode in direct contact with the MIM dielectric must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance." In response, Applicants have amended FIGs. 2D, 2E, 2F, 4C, 4D, 4E, 5C, 5D, 5E, 5F, 6D, 6E, 6F, 7D, 7E and 7F, without adding new matter, by modifying the leaders of top electrodes reference numerals on the aforementioned drawing figures to incorporate all three conductive layers of the top electrodes. This modification was discussed with the Examiner in a phone interview on August 16, 2004 and the Examiner indicated that this modification of the drawings would be acceptable.

The Examiner rejected claims 1, 2, 4, 5-8, 14, 15, 17-24 under 35 U.S.C. 112, first paragraph, for failing to comply with the enablement requirement.

The Examiner rejected claims 4, 5, 17, and 18 under 35 U.S.C. 112, fourth paragraph, for not incorporating by reference all limitations of the claim to which it refers.

The Examiner rejected claimss 1, 2, 14, 15 and 20 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,734,489 to Morimoto et al.

The Examiner rejected claims 6 and 19 under 35 U.S.C. 103 as being unpatentable over Morimoto et al.

The Examiner rejected claims 8 and 21 under 35 U.S.C. 103 as being unpatentable over U.S. Patent Application Publication 2003/0032234 to Suzuki.

Applicants respectfully traverse the §112 and §102(e) rejections with the following arguments.

35 USC § 112

The Examiner rejected claims 1, 2, 4, 5-8, 14, 15, 17-24 under 35 U.S.C §112, first paragraph stating: "The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1 and 14 recited the limitation that the top electrode is in direct contact with the top surface of said MIM dielectric, but Figures 5A-F does not teach this and neither does the specification. Figure 5A-F does not label the layer that is in between the top electrode # 438A2 and the MIM dielectric #436A, but in Figure 1A the intermediate layer is labeled properly. Figure 1 teaches the intermediate layer #160 to be made out of TiN or TaN and that this layer is utilized in all embodiments of the invention, (Applicant's Specification Paragraph 0019 Lines 12-15); thus not enabling."

In response, Applicants respectively point out that reference numeral 160 is described in paragraph [0018] of Applicants specification as an optional portion of top electrode 140 not an intermediate layer. Applicants quote from paragraph [0018]: "Top electrode 140 includes a core conductor 155, an optional bottom conductor 160 and an optional top conductor 165."

Further, Applicants believe that the amendment of FIGs. 5C, 5D, 5E and 5F and paragraph [0038] now clearly indicate to one skilled in the art that the un-referenced layer between top electrode 438A and MIM dielectric 436A is one of three layers making up the top electrode 438A2 and thus there is no intervening layer between top electrode 438A2 and MIM dielectric 436A.

The Examiner rejected claims 4, 5, 17, and 18 under 35 U.S.C. 112, fourth paragraph, for not incorporating by reference all limitations of the claim to which it refers stating: "Claims 4 and 17 do not reference the limitation in the independent claims 1 and 14 that the bottom copper electrode is co-planar with the top surface of the interlevel dielectric, where claims 4 and 17 teach an additional diffusion layer is co-planar with the interlevel dielectric, and where is later taught in claims 5 and 18 that this layer isn't made out of copper either."

In response, Applicants respectfully contend that the cancellation of claims 4 and 17 and the amendments to claims 5 and 18 have made this rejection moot in that amended claim 5 references all limitations of amended claim 1 and that amended claim 18 references all limitations of amended claim 14.

35 USC § 102

As to claim 1, the Examiner states that "Referring to claim 1, an electronic device, (insofar as to understand the claims from the 112 rejections), comprising: an interlevel dielectric layer, (Figure 55 #15), formed on a semiconductor substrate, (Figure 1 #1); a copper bottom electrode, (Figure 55 #30 & Col. 14 Line 7), formed in said interlevel dielectric layer, (Figure 55 #15), a top surface of said bottom electrode co-planer with a top surface of said interlevel dielectric layer, (Figure 55 #152); a conductive diffusion barrier, (Figure 55 #44), in direct contact with said top surface of said bottom electrode, (Figure 55 #30); a MIM dielectric, (Figure 55 #45), in direct contact with a top surface of said conductive diffusion barrier, (Figure 55 #44); and a top electrode, (Figure 55 #33), in direct contact with a top surface of said MIM dielectric, (Figure 55 #45).

Applicants contend that claim 1 is not anticipated by Morimoto et al. because Morimoto et al. does not teach each and every feature of amended claim 1. As a first example Morimoto et al. does not teach "a copper bottom electrode formed in said interlevel dielectric layer, a top surface of said copper bottom electrode recessed below a top surface of said interlevel dielectric layer." Applicants respectfully point out that in Morimoto et al. FIG. 55, metal film 30 is co-planar with and not recessed below the top surface of insulating film 15. As a second example, Morimoto et al. does not teach or suggest "a first conductive diffusion barrier formed on a top surface of said copper bottom electrode, a top surface of said first conductive diffusion barrier co-planar with said top surface of said interlevel dielectric layer." Applicants respectfully point out that in Morimoto et al. FIG. 55, metal film 44 is formed on top surface of insulating film 15. As a third example, Morimoto et al. does not teach or suggest "a second conductive diffusion barrier in direct contact with said top surface of said first conductive diffusion barrier." Applicants respectfully point out that there is no second conductive diffusion barrier taught in Morimoto et al. FIG. 55.

Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Morimoto et al. and is in condition for allowance. Since claims 1, 2, 3, 5, 7, 8, 31 and 32 depend from claim 1, Applicants respectfully maintain that claims 1, 2, 5, 7, 31 and 32 are likewise in condition for allowance.

As to claim 14, the Examiner states that "Referring to claim 14, a method of fabricating an electronic device, (insofar as to understand the claims from the 112 rejections), comprising: (a) providing a semiconductor substrate, (Figure 1 #1), (b) forming an interlevel dielectric layer, (Figure 55 #15), on said semiconductor substrate, (Figure 1 #1);(c) forming a copper bottom electrode, (Figure 55 #30 & Col. 14 Line 7), in said interlevel dielectric layer, (Figure 55 #15), a

top surface of said bottom electrode, (Figure 55 #30), co-planer with a top surface of said interlevel dielectric layer; (d) forming a conductive diffusion barrier, (Figure 55 #44), in direct contact with said top surface of said bottom electrode, (Figure 55 #30); (e) forming a MIM dielectric, (Figure 55 #45), in direct contact with a top surface of said conductive diffusion barrier, (Figure 55 #44); and (f) forming a top electrode, (Figure 55 #33), in direct contact with a top surface of said MIM dielectric, (Figure 55 #45).

Applicants contend that claim 14 is not anticipated by Morimoto et al. because Morimoto et al. does not teach each and every feature of amended claim 14. As a first example Morimoto et al. does not teach "(c) forming a copper bottom electrode in said interlevel dielectric layer, a top surface of said copper bottom electrode recessed below a top surface of said interlevel dielectric layer." As a second example Morimoto et al. does not teach "(d) forming a first conductive diffusion barrier in direct contact with said top surface of said copper bottom electrode, a top surface of said first conductive diffusion barrier co-planar with said top surface of said interlevel dielectric layer." As a third example Morimoto et al. does not teach "(e) forming a second conductive diffusion barrier on a top surface of said first conductive diffusion barrier." Applicants, maintain that the arguments presented supra in respect to claim 1 are applicable to claim 14.

Based on the preceding arguments, Applicants respectfully maintain that claim 14 is not unpatentable over Morimoto et al. and is in condition for allowance. Since claims 15, 18, 20-24 , 33 and 34 depend from claim 14, Applicants respectfully maintain that claims 15, 18, 20-24 , 33 and 34 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that claims X-Z meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below.

Respectfully submitted,
FOR:

Dated: 08/20/2004

BY: Jack P. Friedman
Jack P. Friedman
Reg. No. 44,688
FOR:
Anthony M. Palagonia
Registration No.: 41,237

3 Lear Jet Lane, Suite 201
Schmeiser, Olsen & Watts
Latham, New York 12110
(518) 220-1850
Agent Direct Dial Number: (802)-899-5460